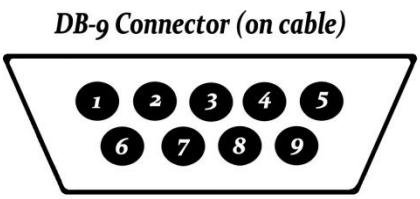
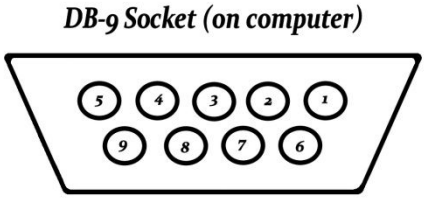
Apple II Family of Computers
Various Connector Pinouts

PDF Prepared by Dr. Kenneth Buchholz
Apple2Online.com
From a Variety of Online Sources

11 July 2013

Apple 300/1200 Modem





Pin	Name	Description
1	n/c	Not connected
2	DSR	Data Set Ready
3	GND	Ground
4	n/c	Not connected
5	RxD	Receive Data
6	DTR	Data Terminal Ready
7	DCD	Output from modem
8	GND	Ground
9	TxD	Transmit Data

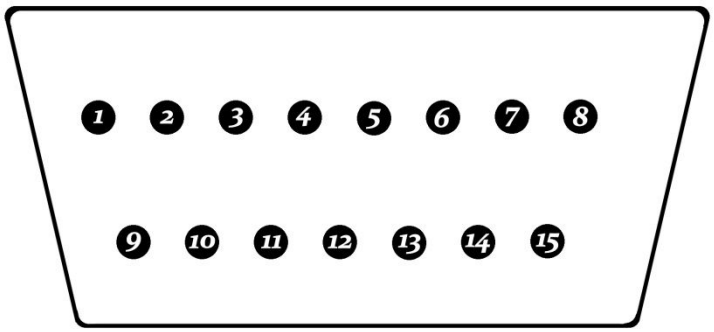
Apple II Slot – 50-pin Female Edge Connector

Pin	Name	Description
1	IOSEC	I/O Select. (No Connection on Slot 0)
2	A0	Buffered Address Bus
3	A1	Buffered Address Bus
4	A2	Buffered Address Bus
5	A3	Buffered Address Bus
6	A4	Buffered Address Bus
7	A5	Buffered Address Bus
8	A6	Buffered Address Bus
9	A7	Buffered Address Bus
10	A8	Buffered Address Bus
11	A9	Buffered Address Bus
12	A10	Buffered Address Bus
13	A11	Buffered Address Bus
14	A12	Buffered Address Bus
15	A13	Buffered Address Bus
16	A14	Buffered Address Bus
17	A15	Buffered Address Bus
18	RW	Buffered Read/Write
19	SYNC	SYNC from Video Generator (Slot 7 ONLY) Not on Rev 0 Motherboards. Used as test pin on Slot 1 for IIe.
20	IOSTRB	I/O Strobe
21	RDY	
22	DMA	
23	INTOUT	Daisy-chain interrupt output to lower priority devices
24	DMAOUT	Daisy-chain DMA output to lower priority devices
25	+5V	+5 Volts power supply, 500 mA max for all boards
26	GND	Ground
27	DMAIN	Daisy-chained DMA input from higher priority devices
28	INTIN	Daisy-chained interrupt input from higher priority devices
29	NMI	No-Maskable Interrupt
30	IRQ	Interrupt ReQuest
31	RES	RESet
32	INH	INHibits the onboard ROMs
33	-12V	-12 Volts power 200 mA max all boards
34	-5V	-5 Volts power, 200 mA max all boards
35	COLORREF	3.5 MHz Video COLOR REF, slot 7 ONLY; Not on Rev 0 Motherboards; Functions as test pin on Slot 1 for IIe.
36	7M	7 MHz clock
37	Q3	2 MHz Asymmetrical Clock
38	PHI1	1 MHz Phase 1 Clock
39	Various	USER1 on Apple II; disable address decode; 65C02 SYNC on Apple IIe; M2SEL on IIGS
40	PHI0	1 MHz Phase 0 Clock (Inverted PHI1)
41	DEVSEL	DEVice SELect
42	D7	Buffered bi-directional data bus
43	D6	Buffered bi-directional data bus
44	D5	Buffered bi-directional data bus
45	D4	Buffered bi-directional data bus
46	D3	Buffered bi-directional data bus
47	D2	Buffered bi-directional data bus
48	D1	Buffered bi-directional data bus
49	D0	Buffered bi-directional data bus
50	12V	+12 Volts power, 250 mA all boards

Apple IIe – 50-pin Female Edge Connector

Pin	Name	Description
1	IOSEC	I/O Select. (No Connection on Slot 0)
2	DMA	DMA In
3	INTIN	Daisy-chained interrupt input from higher priority devices
4	NMI	No-Maskable Interrupt
5	IRQ	Interrupt ReQuest
6	RES	RESet
7	INH	INHibits the onboard ROMs
8	-12V	-12 Volts power 200 mA max all boards
9	-5V	-5 Volts power, 200 mA max all boards
10		No connection
11	7M	7 MHz clock
12	Q3	2 MHz Asymmetrical Clock
13	CLK1	Clock 1
14	USR1	User 1
15	CLK0	Clock 0
16	DEVSEL	DEVice SELect
17	D7	Buffered bi-directional data bus
18	D6	Buffered bi-directional data bus
19	D5	Buffered bi-directional data bus
20	D4	Buffered bi-directional data bus
21	D3	Buffered bi-directional data bus
22	D2	Buffered bi-directional data bus
23	D1	Buffered bi-directional data bus
24	D0	Buffered bi-directional data bus
25	+12V	+12 Volts power supply
26	+5V	+5 Volts power supply, 500 mA max for all boards
27	DMAOUT	Daisy-chain DMA output to lower priority devices
28	INTOUT	Daisy-chain interrupt output to lower priority devices
29	DMA	
30	RDY	
31	STRB	Strobe
32		No connection
33	RW	Buffered Read/Write
34	A15	Buffered Address Bus
35	A14	Buffered Address Bus
36	A13	Buffered Address Bus
37	A12	Buffered Address Bus
38	A11	Buffered Address Bus
39	A10	Buffered Address Bus
40	A9	Buffered Address Bus
41	A8	Buffered Address Bus
42	A7	Buffered Address Bus
43	A6	Buffered Address Bus
44	A5	Buffered Address Bus
45	A4	Buffered Address Bus
46	A3	Buffered Address Bus
47	A2	Buffered Address Bus
48	A1	Buffered Address Bus
49	A0	Buffered Address Bus
50	IOSEC	I/O Select. (No Connection on Slot 0)

Apple II Video Connector



Pin	Name	Description
1	TEXT	Video text signal from TMG; set to inverse of GR, except in double high-resolution mode.
2	14M	14M master timing signal from the system oscillator.
3	SYNC*	Displays horizontal and vertical synchronization signal from IOU pin 39.
4	SEGB	Displays vertical counter bit from IOU pin 4; in text mode, indicates second low-order vertical counter; in graphics mode, indicates low-resolution.
5	1VSOUND	One-volt sound signal from pin 5 of the audio hybrid circuit (AUD).
6	LDPS*	Video shift-register load enable from pin 12 of TMG.
7	WNDW*	Active area display blanking; includes both horizontal and vertical blanking.
8	+12V	Regulated +12 volts DC; can drive 300mA.
9	PRAS*	RAM row-address strobe from TMG pin 19.
10	GR	Graphics mode enable from IOU pin 2.
11	SEROUT*	Serialized character generator output from pin 1 of the 74LS166 shift register.
12	NTSC	Composite NTSC video signal from VID hybrid chip.
13	GND	Ground reference and supply.
14	VIDD7	From 74LS374 video latch; causes half-dot shift high.
15	CREF	Color reference signal from TMG pin 3; 3.58 MHz.

Notes:

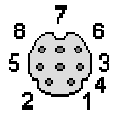
Signals at the DB-15 socket on the Apple IIc are not the same as those at the DB-15 end of the Apple IIGS, Apple III and Macintosh II. Do not attempt to plug a cable intended for one into the other!

Several of these signals, such as the 14 MHz, must be buffered within about 4 inches of the back panel connector, preferably inside a container directly connected to the back panel of the computer.

Apple IIc to Imagewriter II Printer

This cable will allow you to connect the Apple IIc to the Apple Imagewriter II printer.

5 pin DIN female connector
at the computer



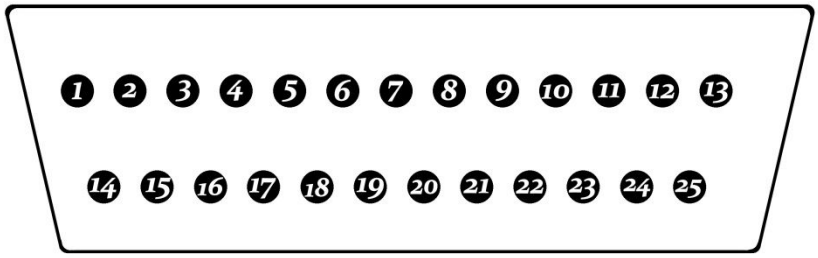
8 pin mini-DIN female connector
at the printer

Device 1 DIN Pin Number	Device 1 Apple Pin Number *	Device1 Pin Name	Direction	Device 2 Pin Number	Device 2 Pin Name	Description (may be empty)
1	1	HSKo	→	2	HSKi	Handshaking
4	2	TxD	→	5	RxD-	Data
2	3	GND		4,8	GND,RxD+	Ground
5	4	RxD	←	3	TxD-	Data
3	5	HSKi	←	1	HSKo	Handshaking

The Imagewriter's pin 6 and 7 are not used. This is equivalent to the Apple IIc Peripheral-8 Cable (A2C4312.)

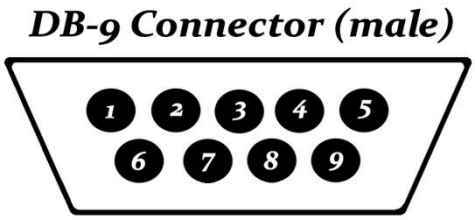
* Please note: Apple's numbering scheme for its' DIN-5 ports do not follow the DIN specification. Both are provided for convenience.

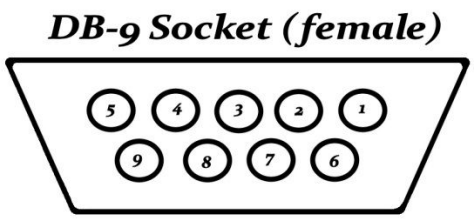
Apple ImageWriter Serial Connector



Pin	Name	Description
1	GND	Ground
2	SD	Send Data
3	RD	Receive Data
4	RTS	Request to Send
7	GND	Ground
14	FAULT-	False when Deselected
20	DTR	Data Terminal Ready

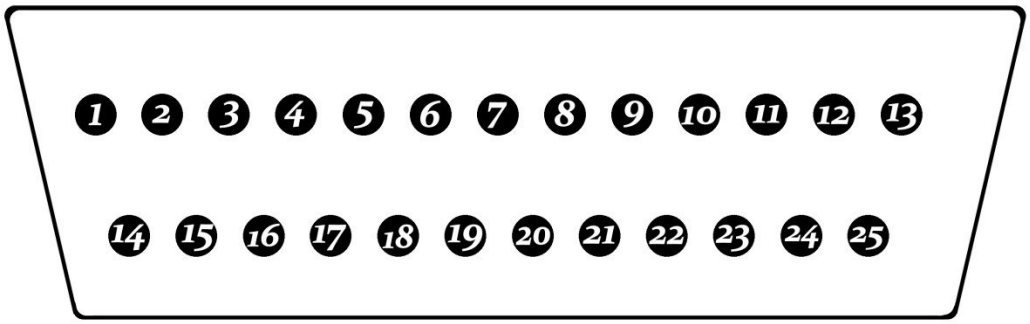
Apple LaserWriter AppleTalk





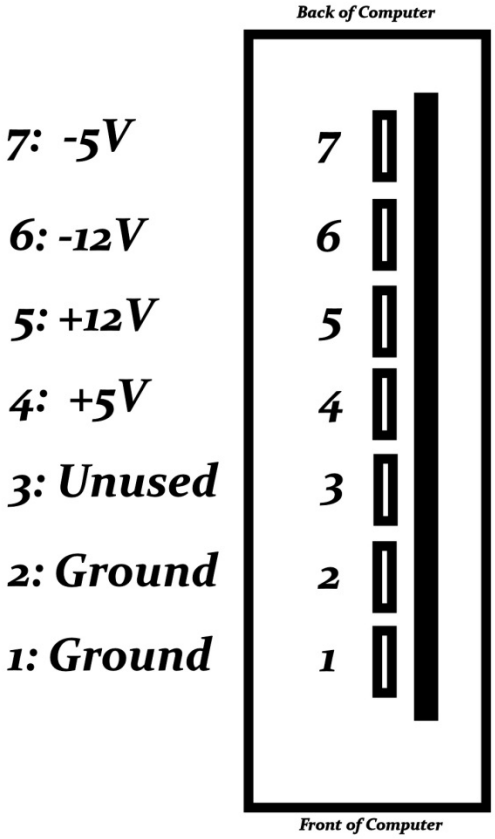
Pin	Name	Description
1	GND	Ground
2		No Connection
3	GND	Ground
4	TXD+	Transmit Data +
5	TXD-	Transmit Data -
6		No Connection
7	RXCLK	TRxC of Zilog 8530
8	RXD+	Receive Data +
9	RXD-	Receive Data -

Apple LaserWriter Serial Connector

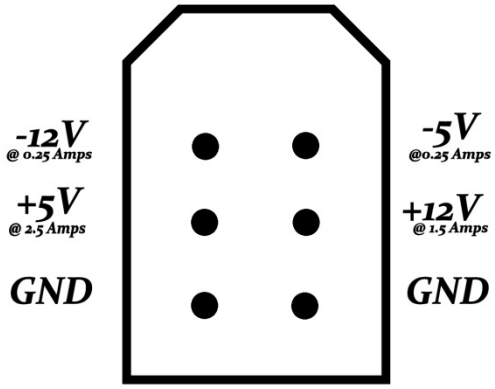


Pin	Name	Description
1	GND	Ground
2	TXD	Transmit Data
3	RXD	Receive Data
4	RTS	Request to Send
5	CTS	Clear to Send
6	DSR	Data Set Ready
7	GND	Ground
8	DCD	Data Carrier Detect
20	DCT	Data Terminal Ready
22	RING	

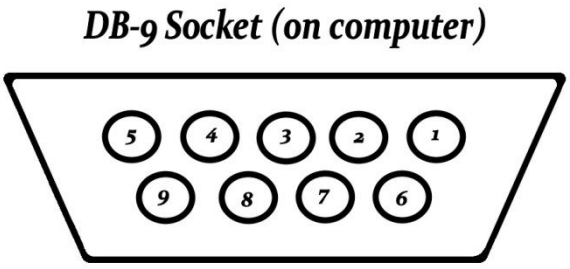
GS Motherboard Power Connector



Apple II+/IIe Power Supply Socket



Apple Game Port (9-pin connector)

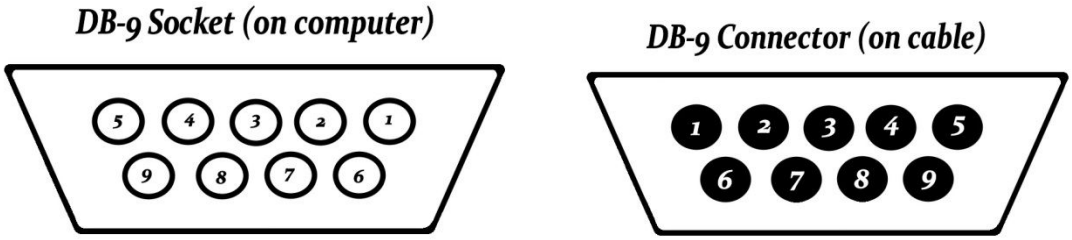


Pin 1: Pushbutton 1
Pin 2: +5V Power
Pin 3: Ground
Pin 4: Game Control2 or Paddle 2 (Joystick-2 X-axis)*
Pin 5: Game Controlo or Paddle o (Joystick-o X-axis)
Pin 6: Pushbutton 2*
Pin 7: Pushbuttono (usually the “Fire” button)
Pin 8: Game Control1 or Paddle 1 (Joystick-1 Y-axis)
Pin 9: Game Control3 or Paddle 3 (Joystick-2 Y-axis)

*Note: These functions are not available on the IIc or IIc+

II, IIc & Laser 128 Mouse

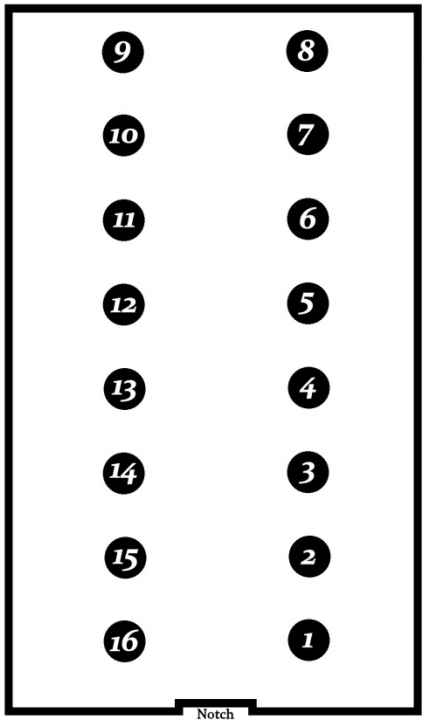
The IIe/IIc mouse can plug into the IIc / IIc+ Game/Mouse port, or on a IIe, into the 9-pin socket of a Mouse Card. When plugged into the IIc or IIc+, several pins are redefined for use with a mouse.



Pin #	Mouse	Computer
Pin 1:	Mouse ID	Pushbutton 1
Pin 2:	+5V Power	+5V Power
Pin 3:	Ground	Ground
Pin 4:	XDIR	No function on IIc, IIc+
Pin 5:	XMOVE	Game/Paddle 0 (Joystick X-axis)
Pin 6:	n.c.	No function on IIc, IIc+
Pin 7:	Mouse Button	Pushbutton 0
Pin 8:	YDIR	Game/Paddle 1 (Joystick Y-axis)
Pin 9:	YMOVE	No function on IIc, IIc+

Apple 16-pin DIP Game Port socket

(on the II, II+, IIe, IIGS motherboard)



Function	Pin
Pushbutton 3 (GS only)	9
Game Controller 1	10
Game Controller 3	11
Annunciator 3	12
Annunciator 2	13
Annunciator 1	14
Annunciator 0	15
No Connection	16

Pin	Function
8	Ground
7	Game Controller 2
6	Game Controller 0
5	/$C040 Strobe
4	Pushbutton 2
3	Pushbutton 1
2	Pushbutton 0
1	+5V Power

Notes:
Game Port Information (with BASIC Peek/Poke locations) obtained from pages 430-433 of the Apple // User's Guide, Second Edition by Lon Poole:

-16296 Annunciator 0 Off
Turns off game control output (annunciator) number 0. The voltage on pin 15 of the game control is set to approximately 0 volts (TTL low).

-16295 Annunciator 0 On
Turns on game control output (annunciator) number 0. The voltage on pin 15 of the game control is set to approximately +5 volts (TTL high).

The following annunciator soft switches follow the same rules as annunciator 0 for their respective pin assignments:

-16294 Annunciator 1 Off
-16293 Annunciator 1 On
-16292 Annunciator 2 Off
-16291 Annunciator 2 On

-16290 Annunciator 3 Off
-16289 Annunciator 3 On

-16287 Read Pushbutton 0
When the pushbutton on game control number 0 or the open-apple key is being pressed, the value in this location exceeds 127. When it is not being pressed, the value is 127 or less.

The following pushbutton soft switches follow the same rules as pushbutton 0 for their respective pin assignments:

-16286 Read Pushbutton 1
-16285 Read Pushbutton 2

-16320 Stobe Output
Normally pin 5 of the game control connector is +5 volts. If you PEEK memory location -16320, it drops to 0 volts for one-half microsecond. POKE will trigger the strobe twice.

The following is a direct excerpt from page 167 of the Apple //e Reference Manual:

> *"The hand-control inputs are connected to the timing inputs of an NE558 quadruple 555-type analog timer. Addressing $C07x sends a signal from the 74LS154 that resets all four timers and causes their outputs to go one (high). A variable resistance of up to 150K ohms connected between one of these inputs and the +5V supply controls the charging time of one of four 0.022-microfarad capacitors. When the voltage on the capacitor passes a certain threshhold, the output of the NE558 changes back to zero (low).*
>
> *Programs can determine the setting of a variable resistor by resetting the timers and then counting time until the selected timer input changes from high to low. The resulting count is proportional to the resistance."*

Basically, the above excerpt is a long description of the BASIC PDL() function.

Apple II Joystick

9-pin Male Connector	Function	16-pin IC-style Connector
Pin 2	+5V	Pin 1
Pin 7	Button 0	Pin 2
Pin 5	X-axis	Pin 6
Pin 8	Y-axis	Pin 10
Pin 1	Button 1	Pin 3
Pin 3	Ground	Pin 8

Apple //e Expansion Slot Pinout

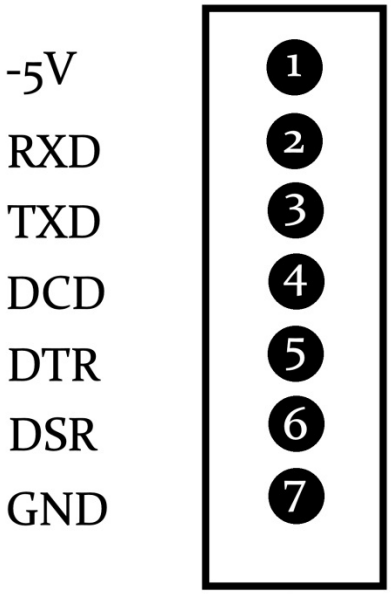
(Card slots, not memory slot)

The following information is from pages 172-174 of the Apple //e Reference Manual regarding the pinout of the expansion slots. (A leading "~" to indicates an active Low signal.)

Pin(s)	Function
1	I/O SELECT - Normally high; goes low during phase 0 when the 6502 addresses location $CnXX, where n is the connector number. This line can drive 10 LS TTL loads.*
2-17	A0-A15 - Three-state address bus. The address becomes valid during phase 1 and remains valid during phase 0. Each address line can drive 5 LS TTL loads.*
18	R/~W - Buffered read/write line. Valid at the same time as the address bus; high during a read cycle, low during a write cycle. It can drive 2 LS TTL loads.*
19	~SYNC - Composite horizontal and vertical sync, on expansion slot 7 ONLY. This line can drive 2 LS TTL loads.*
20	~I/O STROBE - Normally high; goes low during phase 0 when the 6502 addresses a location between $C800 and $CFFF. This line can drive 4 LS TTL loads.*
21	RDY - Input to the 6502. Pulling this line low during phase 1 halts the 6502 with the address bus holding the address of the location currently being fetched. This line has a 3300 ohm pullup resistor to +5V.
22	~DMA - Input to the address bus buffers. Pulling this line low during phase 1 disconnects the 6502 from the address bus. This line has a 3300 ohm pullup resistor to +5V.
23	INT OUT - Interrupt priority daisy-chain output. Usually connected to pin 28 (INT IN). Note: On slot 7 ONLY, this pin can be connected to the graphics-mode signal GR. (Not available on Rev A boards).
24	DMA OUT - DMA priority daisy-chain output. Usually connected to pin 22 (DMA IN).
25	+5V - +5V power supply. A total of 500mA is available for all accessory cards.
26	GND - System common ground.
27	DMA IN - DMA priority daisy-chain input. Usually connected to pin 24 (DMA OUT).
28	INT IN - Interrupt priority daisy-chain input. Usually connected to pin 23 (INT OUT).
29	~NMI - Non-maskable interrupt to 6502. Pulling this line low starts an interrupt cycle with the interrupt-handling routine at location $03FB. This line has a 3300 ohm pullup resistor to +5V.
30	~IRQ - Interrupt request to 6502. Pulling this line low starts an interrupt cycle only if the interrupt-disable (I) flag in the 6502 is not set. Uses the interrupt-handling routine at location $03FE. This line has a 3300 ohm pullup resistor to +5V.
31	~RES - Pulling this line low initiates a reset routine.
32	~INH - Pulling this line low during phase 1 inhibits (disables) the memory on the main circuit board. This line has a 3300 ohm pullup resistor to +5V.
33	-12V power supply. A total of 200mA is available for all accessory cards.
34	-5V power supply. A total of 200mA is available for all accessory cards.
35	3.58MHz color reference signal, on slot 7 ONLY. This line can drive 2 LS TTL loads.*
36	7M - System 7MHz clock. This line can drive 2 LS TTL loads.*
37	Q3 - System 2MHz asymmetrical clock. This line can drive 2 LS TTL loads.*
38	PHASE1 - 6502 phase 1 clock. This line can drive 2 LS TTL loads.*
39	uPSYNC - The 6502 signals an operand fetch by driving this line high during the first read cycle of each instruction.
40	PHASE0 - 6502 phase 0 clock. This line can drive 2 LS TTL loads.*
41	~DEVICE SELECT - Normally high; goes low during phase 0 then the 6502 addresses location $ConX, where n is the connector number plus 8. This line can drive 10 LS TTL loads.*
42-49	D0-D7 - Three-state buffered bi-directional data bus. Data becomes valid during phase 0 high and remains valid until phase 0 goes low. Each data line can drive one LS TTL load.*
50	+12V power supply. A total of 250mA is available for all accessory cards.

* ***Loading limits are for each card.***

Apple IIc+ internal modem connector

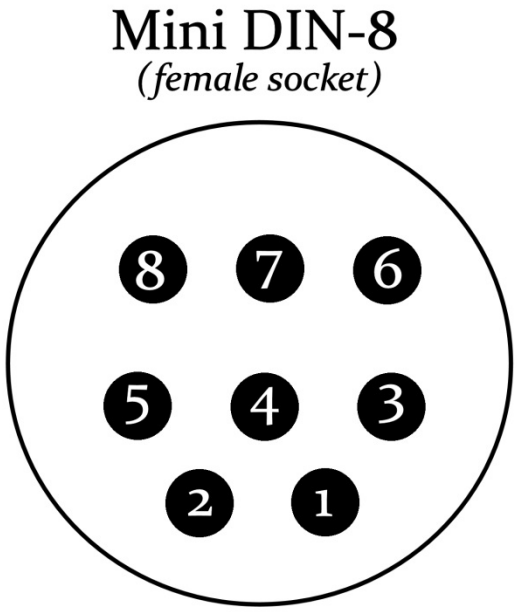


Pin	Function	Description
1	-5V	-5V
2	RXD	Receive Data
3	TXD	Transmit Data
4	DCD	Data Carrier Detect
5	DTR	Data Terminal Ready
6	DSR	Data Signal Ready
7	GND	Ground

IIc+ and IIgs Serial Port

(Mini DIN-8)

View of the IIGS Serial Port from back of computer



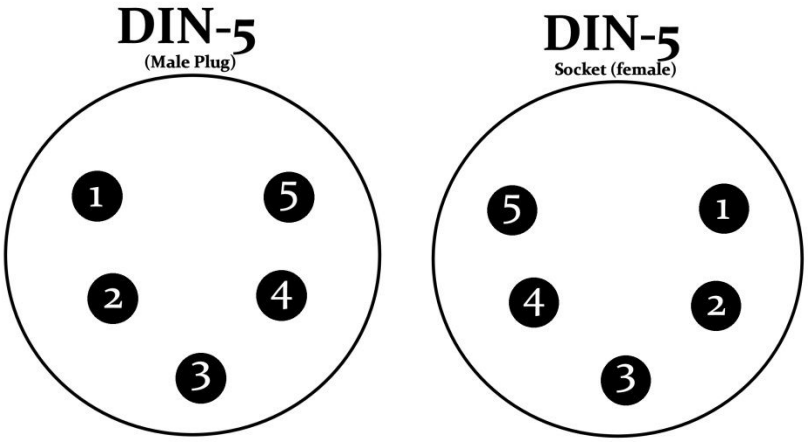
Pin	Function	Description
1	HSKo	Handshake Output
2	HSKi	Handshake Input or External Clock
3	TxD	Transmit Data
4	GND	Signal Ground
5	RxD	Receive Data
6	TxD+	Transmit Data
7	GPi	General Purpose Input
8	RxD+	Receive Data

Cable to Connect Apple IIGS to a Serial DB-25 printer

IIGS	Function	Serial Printer
Pin 1	Handshake Out	Pin 6 (DSR)
Pin 2	Handshake In	Pin 20 (DTR)
Pin 3	TxD-	Pin 3 (RxD)
Pin 4	GND	Pin 7 (Signal Ground)
Pin 5	RxD-	Pin 2 (TxD)
Pin 6	TxD+	No connection
Pin 7	GPi	No connection
Pin 8	RxD+	Loop to Signal Ground (IIGS Pin 4 or DB-25 Pin 7)

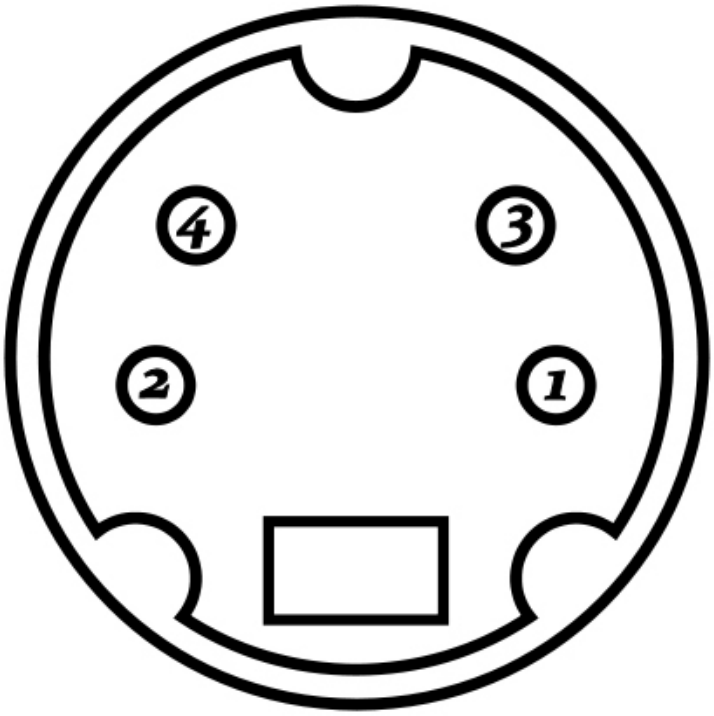
Apple IIc Serial Port (Printer) and Modem Socket

(DIN-5 Connector)



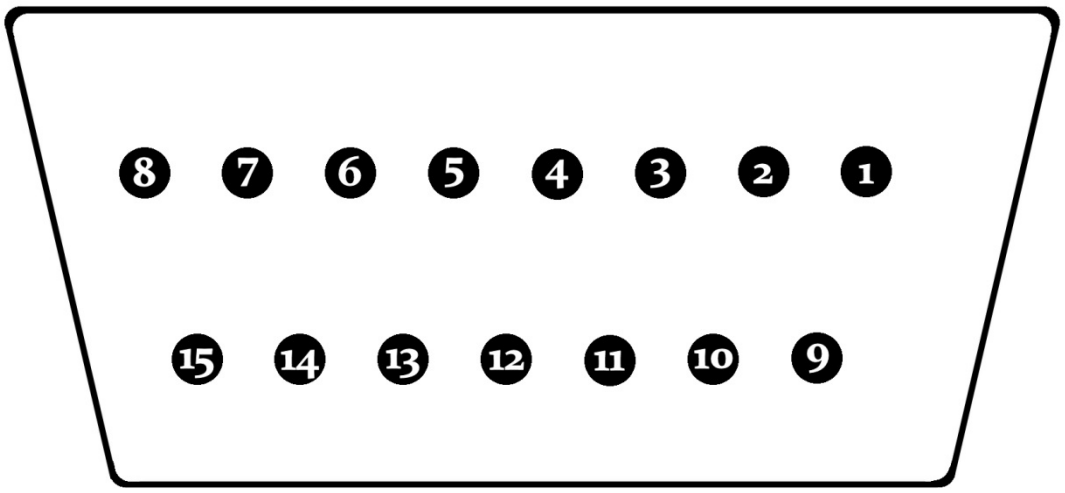
Pin 1	Handshake Out (nominally DTR)
Pin 2	Data Out (TxD)
Pin 3	Ground
Pin 4	Data In (RxD)
Pin 5	Handshake In (nominally DSR)

Apple IIgs ADB (keyboard) socket



Pin	Function
1	Data
2	Reserved
3	+5 Volts
4	Ground

Apple IIGS RGB Socket



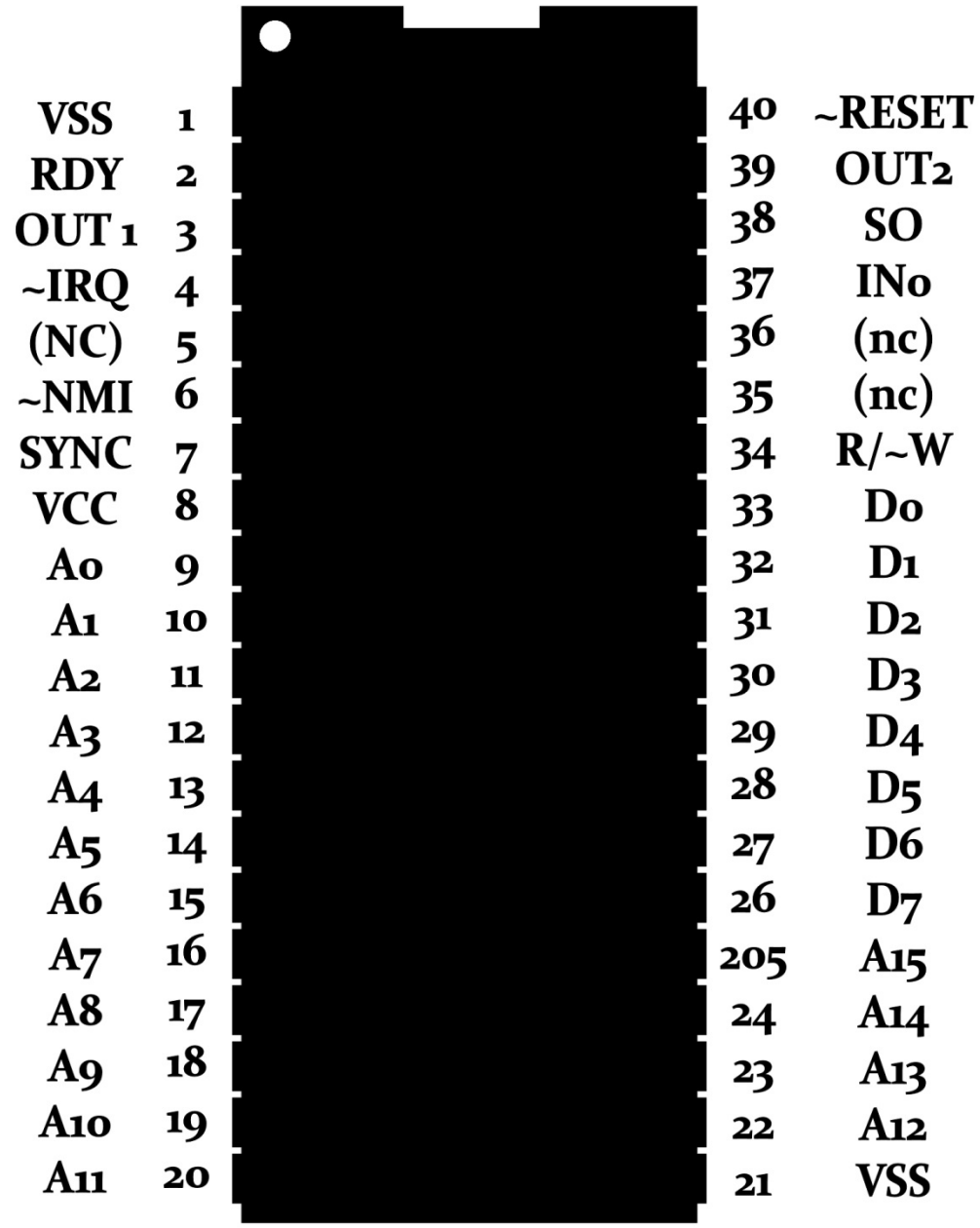
Pin	Signal
Shell	System Ground
1	Ground (red)
2	Red Analog Video
3	Composite Sync
4	Not Used
5	Green Analog Video
6	Ground (green)
7	-5V
8	+12V
9	Blue Analog Video
10	Not Used
11	Audio Output (not used)
12	Composite Video (not used)
13	Ground (blue)
14	Not Used
15	Not Used

Note: "Not used" indicates signals not used by the IIgs RGB monitor.

6502 Microprocessor Pinout

A leading "~" indicates an active Low signal.

Apple 6502 Microprocessor



3.5" and 5.25" Drive Cable

Much of this information comes from page 90 of Open-Apple Volume 1, number 11 (1985).

The following table lists all of the drive control signals for each type of controller card/disk port:

Signal	Function	Unidisk	IIc	IIc+ / IIGS	Disk][
GND	Ground	1-4	1-4	1-3	1, 3, 5, 7
-12V	-12 Volts DC	5	5	5	9
+5V	+5 Volts DC	6, 16	6	6	11, 12
+12V	+12 Volts DC	7, 8	7, 8	7, 8	13, 15, 17, 19
WRPROT	Write Protect	10	10	10	20
PH 0-3	Stepper Motor Phases	11 – 14	11 – 14	11 – 14	2, 4, 6, 8
WREQ	Write Request	15	15	15	10
DRVEN	Drive Enable	17 (9)	17	17 (9)	14
RDDATA	Read Data	18	18	18	16
WRDATA	Write Data	19	19	19	18
EXTINT	External Interrupt	-	9	-	-
3.5DISK	Apple 3.5 Drive Enable	-	-	4	-
HDSEL	3.5 Drive Head Select	-	-	16	-
	(not connected)	-	16	-	-

***Notes*:**

The UniDisk uses pin 9 to select the second drive. Inside each UniDisk, the signal from pin 9 at the computer is connected to pin 17 of the daisy-chain drive connector. When the computer selects drive 2 by activating pin 9, the first drive passes this through and the second drive sees its enable signal on pin 17. Thus all drives are identical.

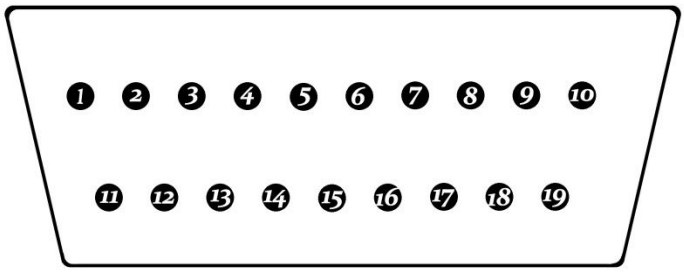
The Disk][controller has two drive connectors, and the same pin (14) is used on each connector to select the appropriate drive. This signal is the only difference between the connectors - all other signals are connected in parallel.

Despite the IIgs having special functions for pins 4 and 16, they may be ignored when dealing with 5.25" drives, and treated as a UniDisk controller (i.e. connect pin 4 to ground, and pin 16 to +5V). The Apple 3.5 drive disconnects these signals internally, so that they will not interfere with its operation.

The UniDisk, IIc external drive and equivalents use a Dsub-19 connector, in which the pins are numbered along the connector, i.e.

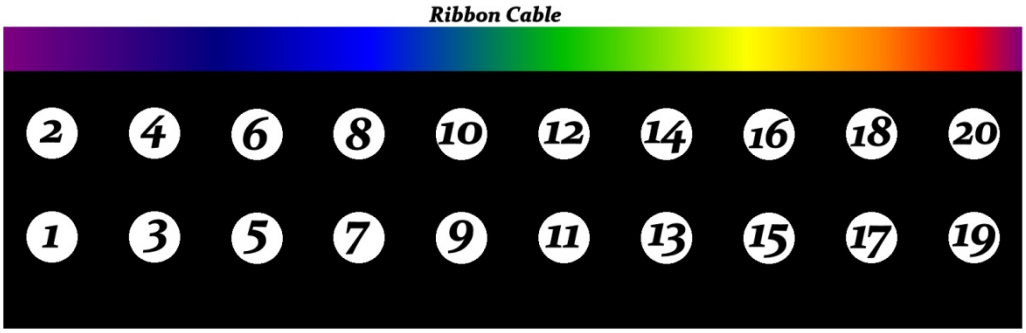
Apple DB-19 Connector

Apple UniDisk & Apple Disk IIc Drives



Apple Disk][IDC-20 Connector

Top View

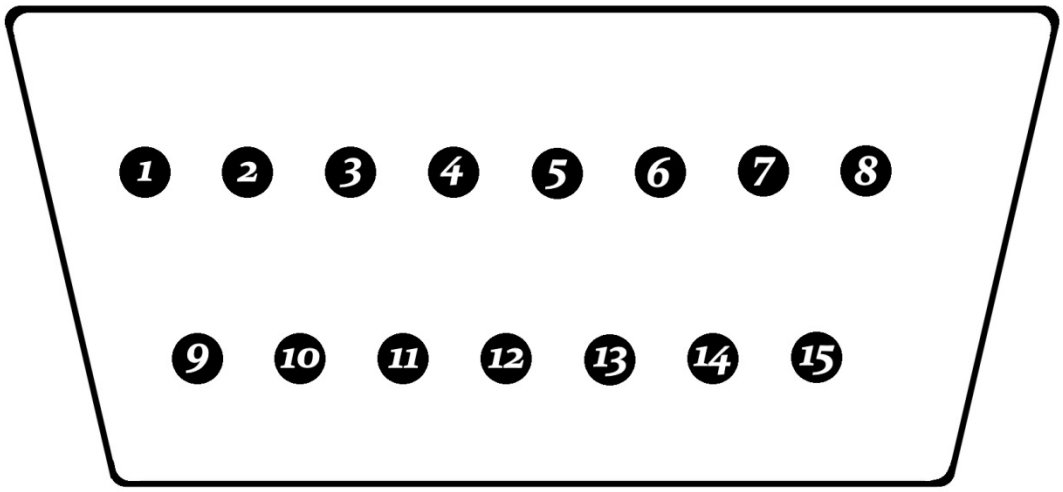


The above diagram is looking at the back of the plug (top side, where ribbon cable connects.

Apple //c DB-15 Video Connector

Source: Apple Computer & Allpinouts.org

Apple IIc Video Connector



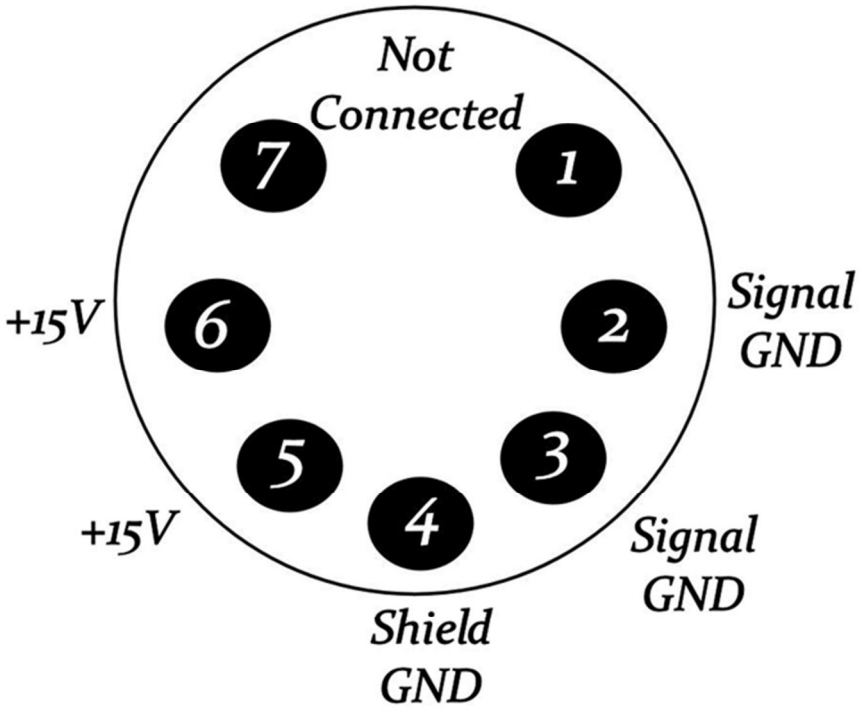
Pin	Signal	Description
1	TEXT	Video text signal from GLU
2	14M	14MHz Timing signal from master oscillator
3	SYNC	Display synchronisation signal from IOU pin 39
4	SEGB	Display Vertical counter bit from IOU pin 4
5	1VSOUND	1v sound signal
6	LDPS	Video shift Register load enable
7	WNDW	Active area display blanking
8	+12v	Regulated +12v
9	PRAS	Ram row address strobe
10	GR	Graphics mode enable
11	SEROUT	Serialized character generator output
12	NTSC	Composite NTSC video signal
13	GND	Ground
14	VIDD7	Causes half dot shift if high
15	CREF	Colour reference signal

Notes:

The signals at the Dsub-15 on the Apple IIc are not the same as those at the Dsub-15 end of the Apple III, Apple IIGS, and Macintosh II. Do not attempt to plug a cable intended for one into the other.

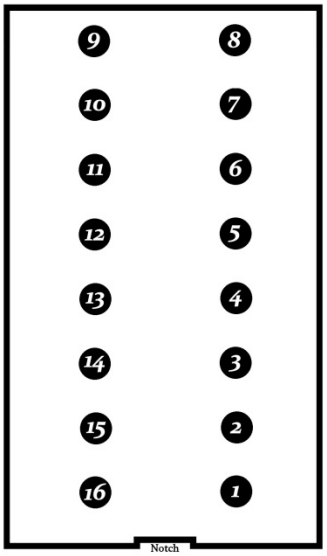
Several of these signals, such as the 14 MHz, must be buffered within about 4 inches of the back panel connector--preferably inside a container directly connected to the back panel.

Apple IIc External Power Connector



Apple II/II+ Keyboard Socket

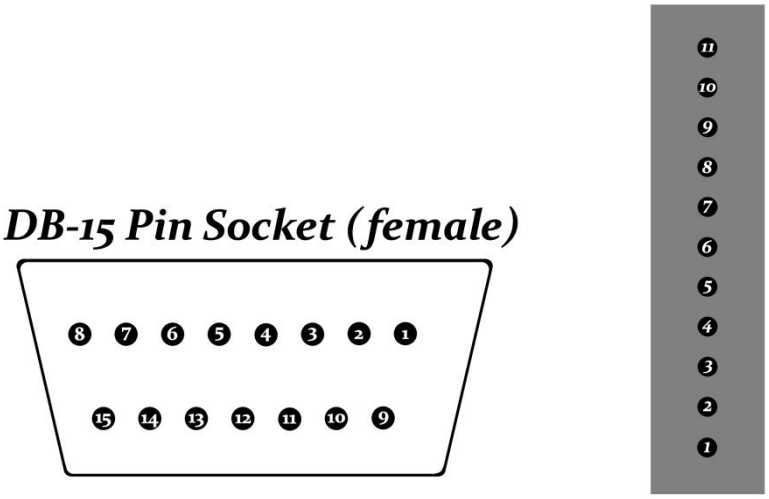
(This socket is located near the front of the motherboard.)



Pin	Name	Description
1	+5V	+5 Volts power; total current drain must be less than 120 mA.
2	Strobe	Strobe output from keyboard. May be of either polarity & pulse should be at least 10 microseconds for each key press.
3	RESET	Microprocessor's RESET line. Normally high, pulled low when RESET key is pressed.
4	NC	No connection
5	DATA	1 of 7 bits ASCII keyboard data input.
6	DATA	1 of 7 bits ASCII keyboard data input.
7	DATA	1 of 7 bits ASCII keyboard data input.
8	GND	System ground.
9	NC	No connection
10	DATA	1 of 7 bits ASCII keyboard data input.
11	DATA	1 of 7 bits ASCII keyboard data input.
12	DATA	1 of 7 bits ASCII keyboard data input.
13	DATA	1 of 7 bits ASCII keyboard data input.
14		
15	-12V	-12 Volts power. Keyboard should draw less than 50 mA.
16	NC	No connection

Apple //e Numeric Keypad Adapter Cable

In order to use a newer numeric keypad with a DB-15 plug (male) on an Apple IIe that only has an 11-pin header on the motherboard for connecting a numeric keypad, you can create an adapter cable as follows:



DB-15 Socket	11-pin Motherboard Header
12	11
11	10
10	9
9	8
(no connection)	7
7	6
6	5
5	4
3	3
2	2
1	1